Redefining the Power Benchmark

Atmel White Paper

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Abstract

This whitepaper discusses the need for low power in high performance MCUs; it looks at how this ultra-low power operation is achieved while maintaining the high performance and features needed in low power applications while, importantly, explaining why engineers need to make themselves aware of the trade-offs and optimizations different IDMs must make in order to achieve ‘low power’.

Introduction

Power consumption is now a high priority at every stage in the entire microelectronics supply-chain. No phase is immune to the demand for better control over power consumption. It can often be seen purely as end-user pressure, but the need to reduce power dissipation at the transistor level has been occupying engineers' minds for a lot longer than the battery life of portable equipment. Before it was comprehensively addressed, power dissipation was threatening to limit transistor integration and thereby stall the progress of integrated circuit design.

The need for engineers to efficiently balance the power budget, however, remains and continues to impost significant demands on the engineering community. Low power techniques and methodologies now exist to address this concern and are employed by every Integrated Device Manufacturer (IDM) in the industry, in one way or another.

ARM®, supplier of the one the most pervasive processor architectures in the semiconductor industry, built its business on designing low power microprocessor cores and has been successful in licensing its IP to the industry. The latest and arguably most successful derivative of the ARM architecture is the Cortex™ family, with three branches addressing specific sectors; the Cortex-A family targets application processors, the Cortex-R branch focuses on real-time requirements, while the Cortex-M range now enables a wide range of powerful but power-conscious 32-bit microcontrollers.

Power consumption is now a high priority at every stage in the entire microelectronics supply-chain. No phase is immune to the demand for better control over power consumption.

However, although designed for low power, the core itself is physically one of the smallest elements of an MCU. And while the core is designed for low power, it isn't safe to assume that all Cortex-M based MCUs offer the same low power performance. As an IP provider, ARM's philosophy isn't to homogenize the market but to empower it, providing each licensee the basis of an MCU but leaving the overall functionality, optimization and differentiation of individual families to the IDM. In this respect, just because a vendor uses a low power core, it doesn't follow that the resulting MCU is truly low power – not all Cortex-M based MCUs are created equal.

This whitepaper discusses the need for low power in high performance MCUs; it looks at how this ultra-low power operation is achieved while maintaining the high performance and features needed in low power applications while, importantly, explaining why engineers need to make themselves aware of the trade-offs and optimizations different IDMs must make in order to achieve 'low power'.

With this backdrop, this paper also introduces the Atmel® SAM4L – Atmel's latest ultra-powerful, ultra-low power MCU made possible by fully understanding how to balance the power budget.

Concepts of Low Power - How Low is Low?

The term 'low power' is now so endemic that it has lost a lot of its impact and some of its meaning. From an MCU manufacturer's point of view, low power is relative to the competition and it should be apparent to engineers that not all Cortex-M4 based MCUs, for example, operate within the same power envelope.

In order to really deliver low power, IDMs must develop their own low power technologies and methodologies, which they can apply to the Cortex-M4 IP. Atmel has devoted many years developing just such a low power solution, its proprietary picoPower®.

While fabless IDMs must use plain vanilla low power processes that are available on the open market, Atmel has developed process technologies that further improve on a generic process. IDMs that are serious about low power MCU design will focus not only on the CPU but the entire system, developing transistor technologies that offer low power and low leakage, but with the flexibility to employ high performance transistor topologies in areas where they are needed most. picoPower delivers this capability.

When an MCU is designed for low power it must deliver across a range of use-cases. Measuring power isn't straightforward under the best of conditions, so being able to rely on the entire architecture to deliver low power operation under all conditions is essential. Benchmarking MCUs for power is largely dependent on two states of operation – static and dynamic. Power is often equated as a function of a constant (capacitance), frequency and voltage, where:

$$P = K * F * V^2$$

This is a somewhat simplified equation but provides a good foundation for evaluating the architecture. Under dynamic conditions, the frequency of operation clearly has an impact, as power is 'nominally' only consumed in a CMOS circuit when there is a logic transition. Reducing the frequency, therefore, lowers the transitions per second, but doesn't address the number of times a transistor must switch in order to achieve a given task. For this, the core's architecture is crucial, which is why the more powerful Cortex-M4 can deliver results faster (fewer operations, and therefore fewer logic gate transitions) than, say, an 8051.

The second part of the equation relates to the supply voltage but is fundamentally geared to the manufacturing process. Voltage has an exponential impact on power consumption. Lowering the supply voltage delivers greater power savings than scaling the frequency alone. Operating from a lower supply voltage isn't as simple as lowering the clock frequency, however. It must be 'designed in' at the process level.

Atmel's family of ARM Cortex-M3 and -M4 MCUs has recently been extended to include the SAM4L, an ultra-low power solution developed using Atmel's picoPower technology …to bring the benefits of the Cortex-M4 core to applications that demand true low power operation.

Static power is consumed when the CMOS gates are supposed to be in a quiescent state (not switching). While this should, in theory, be zero, in practice it is impossible— and more so as process nodes reduce — to create a transistor with no leakage current in modern geometries. In general, the smaller the geometry, the greater the leakage current, therefore, the more transistors integrated in a device the higher the potential altogether in the static leakage current. By developing low leakage transistors, a proprietary process like picoPower can successfully address these issues and maintain the leakage close to the theoretical zero without sacrificing performance.

Concepts of Low Power - Responsiveness

As the fastest and most frequently switching transistors in an MCU will be found in the core's RAM and the core itself, it follows that all the time the core and its sub-system is active it will dissipate the greatest amount of system power.

For this reason, sleep modes are now ubiquitous among MCUs. The Cortex-M4 has been developed by ARM to support two sleep modes, each of which turns off a greater or lesser degree of system clocks. IDMs choose how to implement their own sleep modes but they all essentially require the core to halt and store system-critical information in registers and RAM, ready to be reinstated when exiting sleep mode. This all takes time and in a typical MCU application, time is synonymous with responsiveness.

Because of this, low power goes far beyond the transistor's switching characteristics. It is a direct result of the overall system architecture. Only by approaching the architectural design from this systemic viewpoint can an IDM truly develop a low power solution. Atmel's family of ARM Cortex-M3 and -M4 MCUs has recently been extended to include the SAM4L, an ultra-low power solution developed using Atmel's picoPower technology that integrates numerous low power techniques specifically designed to bring the benefits of the Cortex-M4 core to applications that demand true low power operation.

It features Atmel's proven approach to managing system power, through a distributed peripheral network that operates independently of the system clock, allowing the core to remain in a deep sleep mode for much longer than in competitive Cortex-M4 MCUs.

Concepts of Low Power - A Holistic Approach

By addressing all aspects of power consumption, IDMs are better able to design an MCU that offers true low power operation. Implementing a Cortex-M4 in a low leakage process will, of course, result in lower system power than if it were implemented in a high performance process, but if the system design is entirely core-centric, it is likely that even the most mundane tasks will require the core's intervention. For example, a simple interrupt service routine, even where no action is taken, would require the core, Flash and other system modules to be fully woken from a sleep mode.

With a high performance core like the Cortex-M4, the action of waking the core and its entire sub-system from deep sleep, just to execute a service interrupt routine or some other simple task, would actually take considerably longer than the time needed to process the actual task. This would not only consume a significant amount of valuable system power, but most of it would be used just in waking the system.

It follows that through a holistic approach that adopts low power techniques complementary to the core, an IDM can develop and implement features that make extensive use of low leakage transistors in the core and peripherals while also reducing the time spent processing. Consequently, they can maximize low power operation.

This holistic approach is proving to be the most relevant and effective way for manufacturers to optimize for power. The degree to which it is employed is what really differentiates IDMs within the Cortex-M4 sphere.

A History of Low Power - Active Mode

Before static power became a major factor in system design, active power was possibly the only design parameter that concerned most engineering teams. IDMs like Atmel have a long history of delivering MCUs that offer more performance at lower active power. This legacy isn't by accident.

One aspect of maintaining low active power is finding the most efficient way of moving in and out of sleep modes. The faster the system clock can be re-established, the faster the core can complete its task and the less active power used.

Further to this, Atmel implements features that can operate independently of the core. Intelligent, autonomous peripherals are able to process inputs and outputs independently of the CPU. Running off a dedicated clock, this approach allows the core to remain in sleep mode for longer and through carefully architected inter-communication features, peripherals are also able to exchange data using shared buses, enabling them to make intelligent decisions based on external stimuli without having to wake the core.

Enabling peripherals to operate autonomously is now recognized as a key addition to low power operation. However, it is, again, crucial that the implementation is integral to the overall system architecture. Peripherals that exhibit a fast response time to the point of real-time operation are essential if they are to manage tasks normally handled by a high performance core.

The Peripheral Event System in the SAM4L is truly independent of both the CPU and its clocking system. With its own access control to the real-time clock the Peripheral Event System is able to continue operating when the CPU and the system clock are effectively 'off'. The result is a much greater power saving than if the system clock needed to continue running.

A History of Low Power - picoPower

The ability to fully understand and design for low power can differentiate manufacturers and their MCUs, irrespective of the core used. Experience counts for a lot and Atmel has a long history of developing low power solutions, based on its picoPower technology. This was first used in the 8-bit AVR® family and the latest picoPower technology now enables the SAM4L, becoming the first Cortex-M4 device to feature picoPower.

Perhaps most significant is the supply voltage; for instance, the SAM4L is able to operate down to a true 1.62V without sacrificing any functionality of the core or, more crucially, the peripherals. This is a class-leader. No other Cortex-M4 based MCU available today, from any manufacturer, is able to operate at such a low supply voltage.

The impact of this is simple. Referring back to Equation 1 we can see that the lower the VCC the lower the power. Unlike frequency, which returns a linear decline, the supply voltage has an exponential impact on power, so being able to operate at a true 1.62V makes the SAM4L the lowest power Cortex-M4 solution available.

The Peripheral Event System in the SAM4L is truly independent of both the CPU and its clocking system.

Other features of picoPower technology that help minimize system power include extensive use of intelligent clock gating. As explained earlier, in active mode CMOS consumes most power when changing state, so by avoiding unnecessary logic state changes active power is significantly reduced. Clock gating is widely recognized in the semiconductor industry as an effective low power technique, but its implementation can vary between manufacturers. The right level of clock granularity and an efficient way of determining how to gate those clocks are low level architectural features that need to be fully integrated into the design, as it is with picoPower.

In addition, by developing techniques for ultra low power memory and integrating it into the picoPower methodology, Atmel's MCUs deliver fast, accurate and robust Flash memory that consumes much less power than competing solutions. This is achieved through a unique approach called Flash Sampling, which compares favorably against the standard approach, where the Flash memory is always active. Using Flash Sampling, the memory blocks are only powered for a few ns, just long enough for the control block to sample the memory's contents. The memory blocks are then immediately disabled, thereby keeping active power in the Flash memory to an absolute minimum.

The Evolution of Low Power - Bringing picoPower to the Cortex-M4

As a low power methodology, picoPower is the primary technology used in Atmel's low power MCUs to address the three key areas of power consumption – sleep mode, active mode and wake-up times.

Atmel's first 32-bit device to feature picoPower was the AVR-based UC3L, which set the benchmark for low power MCUs. That benchmark has been further defined by the SAM4L, which takes low power to a new level.

The picoPower technology permeates the entire architecture, from the process technology used to manufacture the device, to the speed at which peripherals and clocks operate. Although conceptually similar to the way it was integrated in to the UC3L, in practice picoPower — as implemented in the SAM4L, which is the first ARM-based 32-bit device from Atmel to employ picoPower — is evolutionary. Consequently, when implementing the methodology in a new family, Atmel's engineers had the chance to introduce improvements, such as extending it to new peripherals, while making further power reductions.

This returns an active mode power consumption that is significantly lower than the competition; 90µA/MHz, which is achieved in part through the development of an ultra-low power buck regulator. Thanks to its low noise immunity and high efficiency, the fully integrated regulator also enables the SAM4L to operate down to 1.62V, while the LDO only consumes 180µA/MHz.
The SAM4L consumes as little as 1.5µA in WAIT mode, with full RAM retention. Bundled with an unrivalled wake-up time of less than 1.5µS, the SAM4L gives the lowest total power consumption. In sleep mode, the SAM4L draws as little as 0.5µA with the Real-Time Clock still running, and with a wake-up time of less than 2µS.

Industry's Highest Efficiency

While manufacturers are apt to quote their best figures in datasheets, there exists an independent industry body that ensures an 'even playing field' is maintained. The CoreMark, developed by the Embedded Processor Benchmark Consortium (EEBMC) provides a standard set of benchmarks that IDMs subscribe to, in order to measure the performance of their MCUs under 'real world' conditions.

In every documented test result, the SAM4L outperforms its competitors, even those based on the latest, lowest power Cortex-M0+. As the SAM4L uses the Cortex-M4, the largest and most powerful of the Cortex-M cores, the results (Table 1) emphasize the impact and importance of developing and implementing an industry-leading low power platform, philosophy and manufacturing capability.

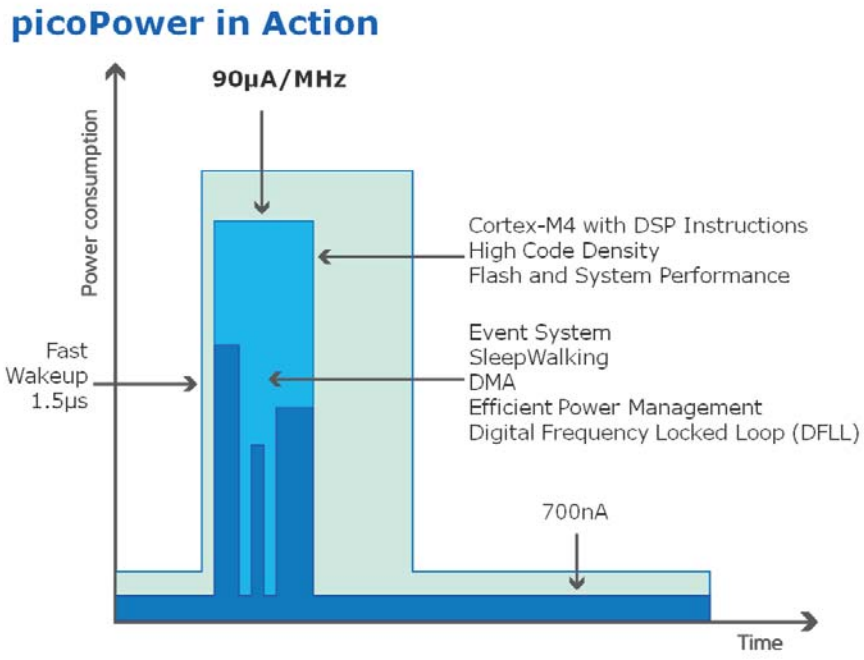

Table 1.

Atmel SAM4L MCUs redefine the power benchmark, delivering the lowest power in both active (90uA/MHz) and sleep modes (1.5uA with full random access memory (RAM) retention and 700nA in backup mode). They are the most efficient MCUs available today, achieving up to 28 CoreMark™/mA using the IAR Embedded Workbench, version 6.40. Atmel SAM4L MCUs also deliver the industry's shortest wakeup time at 1.5us from deep-sleep mode.

The Evolution of Low Power - SleepWalking

In most competitor solutions, responsiveness is directly and inversely linked to system power; it is a simple equation where a faster response time requires greater transistor activity and therefore higher system power. As outlined earlier, Atmel's approach is not to provide low power at the cost of system responsiveness. Here, we take a closer look at how this achieved.

Most manufacturers — Atmel included — must accept that in order to achieve maximum power savings during sleep mode, more of the device needs to be switched 'off'. Waking from deep sleep modes is notoriously costly in terms of the time it takes for the PLLs to stabilize and the number of clock cycles it takes for the system to be fully active. When the task is short, this overhead can easily represent more system power than, say, a simple interrupt service routine.

SleepWalking is a feature that extends the concept of autonomous peripherals that operate independently of the CPU core during active mode, to actually keeping the peripherals functional when the system clock has been stopped. This is achieved by clocking the peripherals using the real-time clock (RTC), instead of the system clock.

In the SAM4L, SleepWalking has been integrated into many of the peripherals, including the analog comparator, the ADC, the I^2C, UART and the capacitive touch interface. It is then the peripheral that

decides whether to wake the system, instead of the CPU waking periodically to carry out an interrupt service routine.

This distributed logic approach allows peripherals to make intelligent decisions; to decide whether or not to wake up the CPU by qualifying an incoming event. This may be a temperature reading from an external sensor, or checking an I^2C address match on a common external bus. The ability to make this level of qualification at the peripheral level can easily reduce the power consumption by a 100-fold in a typical application.

With the SleepWalking integrated in to a larger number of peripherals, the need to wake the CPU reduces significantly, while the ability for peripherals to interact and modify their parameters autonomously, this feature can conceivably allow the CPU to remain inactive for the majority of operational time.

The Evolution of Low Power - Low Voltage Operation

As the only device available on the market that is able to operate down to 1.62V, the SAM4L achieves unprecedented levels of low power operation. A significant contributor to this performance is the integration of two regulators; a buck regulator and an LDO regulator.

The LDO regulator is a conventional solution to regulating an external power source for use inside the device. The buck regulator is more revolutionary, as it reduces the power drawn by the regulator in active mode by around 50%.

The Evolution of Low Power - Balancing Power with Responsiveness

As explained, the key to maintaining lower overall power is ensuring that the amount of time the CPU spends in active mode is kept to a minimum. The Peripheral Event System and, by extension, the SleepWalking features of the SAM4L help deliver the performance needed when the core is in a deep sleep mode, it is inevitable that at some point the core will need to wake up, perform some computations and go back to sleep, and all in as short a time as possible.

A critical element of this process is the phase locked loop (PLL) circuit which powers the system clock. To achieve better performance and accuracy, Atmel has developed a new generation of PLL, the digital frequency locked loop (DFLL). This replaces the traditional PLL with a circuit that can operate over a wider frequency range (8 − 150kHz), start up in just 10µS and lock in 100µS. Furthermore the DFLL can produce an output frequency of between 40 − 150MHz with an accuracy of ±0.1% accuracy over the full temperature and voltage range.

This new design also reduces EMI; as it uses a spread spectrum generator it distributes radiated emissions across multiple frequencies, and features configurable step size, maximum spread and step frequency.

SAM4L – Architecture & Key Features

At the heart of the SAM4L is the ARM Cortex-M4 core; Atmel's first Cortex-M4 device to feature the revolutionary picoPower technology.

As Figure 1 below shows, the core is supported by a number of system features, connected through the Multi-layer High Speed Matrix. What is less obvious from the diagram is the extensive use of dedicated, distributed busses and clocks, all of which can be enabled or disabled, and clocked at different speeds. This fine granularity of bus and clock systems is crucial to maintaining complete control over the peripherals, allowing the user to turn off any peripheral or module that isn't needed at any time and thereby delivering greater control over active and static power consumption.

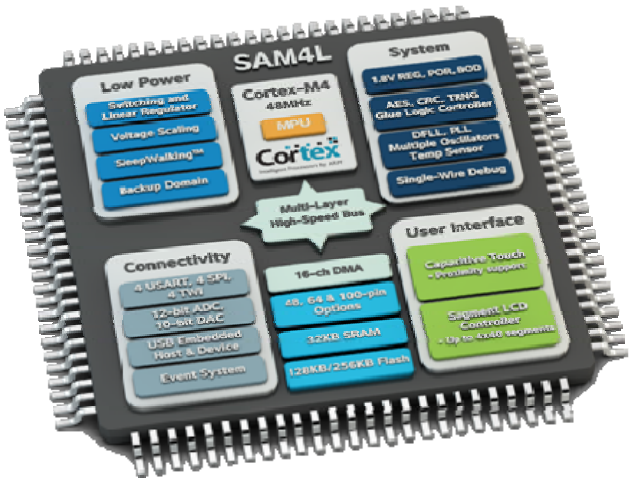

Figure 1. Block diagram of Atmel's SAM4L microcontroller.

In addition, there is the DMA sub-system, which integrates with the High Speed Matrix and the Peripheral Event System. This is what facilitates the message passing between peripherals, with a fixed 2-cycle response.

All of the features in the SAM4L have been developed to deliver the industry's lowest power Cortex-M4 MCU. While the SAM4L's exceptionally low power is attributable to Atmel's picoPower technology, the value of the SAM4L as a microcontroller is due to design elements that make it a truly capable MCU. These can be categorized as either architectural or functional.

Key Architectural Features:

- The latest innovations in picoPower
  - Wait mode with full RAM retention down to 1.5µA
  - Retention mode down to 0.9µA
  - Back-up mode with RTC down to 0.7µA
  - Fast wake-up (1.5µS)

- True 1.6V operation
  - Fully functional, including ADC and Flash, down to 1.62V
  - Flexible voltage supply: 1.8V (regulated) or 1.62 – 3.6V (battery)

- Switching Regulator
  - Down to 100µA/MHz
  - Lower noise immunity
  - Higher efficiency

- Linear Regulator
  - Down to 190µA/MHz
  - High noise immunity
  - Lower efficiency

- Peripheral Event System
  - Precise timing
  - Reduced CPU overhead
  - Reduced power consumption
  - Inter-Peripheral communication - CPU and DMA independent
  - Latency-free event handling
    - Safe fault protection
    - 100% predictable reaction time

- SleepWalking
  - Intelligent peripherals
    - Compare input to preset threshold, and alert CPU when threshold exceeded
    - Reduce CPU overhead by eliminating unnecessary interrupts
    - Reduce power consumption in sleep modes

- RTC/Asynchronous Time (AST)
  - Real-time clock and calendar functionality
  - Any oscillator can be used as a clock source
  - Periodic alarms and time alarms supported
  - Prescaler tick interrupts
    - 60µS to 36 hours with 32kHz input clock
  - Digital tuning for 1ppm accuracy

- Digital Frequency Locked Loop - the next-generation in PLL
  - Replaces traditional PLL
    - Wider input frequency range (8kHz to 150kHz)
    - 10µS start-up

        - 100µS to lock
    - Output frequency 40 to 150MHz
    - ±0.1% accuracy over temperature and voltage range
    - Reduced radiated noise (EMI)

- Frequency Meter
    - Automatically detect failing clocks
    - All clocks can be measured
    - Multiple uses

Key functionality features:

Integrated at the hardware level, the capacitive touch module operates using PCB tracks as sensors. As with other peripherals, this module is linked to the Peripheral Event System and supports SleepWalking mode, which means it can be configured to wake the system based on detecting the proximity of an external element, such as a user's finger passing across an interface panel.

Because it uses capacitance as a trigger, no physical contact is required. By simply defining a button, slider, wheel or landing pad using standard PCB tracking, a sophisticated user interface can be configured that is mechanically isolated from the system. The key features of the capacitive touch panel include:

SAM4L means engineering teams can confidently balance the power budget, without compromising on performance.

- Endless configuration possibilities
- Event driven, including touch, out-of-touch or autonomous interrupts
- Integrated with the Peripheral Event System

In addition to capacitive touch sensing, the SAM4L also integrates an LCD controller that can drive a 4x40 segment display. This too is capable of autonomous operation, offering automatic scrolling, animation and segment/display blinking. When used in conjunction with the capacitive touch sensor module, for example, a message can begin scrolling when a user is detected, before the CPU comes out of sleep mode. The LCD module integrates ASCII character mapping, which further improves the display update rate while reducing power consumption.

Additional key elements of the SAM4L include:

- A 12-bit ADC, capable of 350ksps with programmable gain and programmable sample-and-hold
- A 10-bit DAC, able to sample at 500ksps
- UART, supporting synchronous and asynchronous, RS232, SPI, IrDA, RS422 and RD485
- Full Speed USB host with on-chip transceivers
- True random number generator
- 128-bit AES security module (FIPS 197 compliant)
- Atmel's Glue Logic Controller (GLOC) and PARC modules

Conclusion

When compared with competitive Cortex-M4 based MCUs, preliminary results show the SAM4L consistently out-performs its competition in industry-standard benchmarks such as EEMBC's CoreMark; a measure of how much power a device takes to execute a standard set of functions.
This is no coincidence. picoPower has been continuously developed to provide the industry's leading low power platform and together with further optimizations this has enabled Atmel to deliver the world's lowest power, highest efficiency Cortex-M4 based MCU.

By integrating intelligence at every stage, Atmel's SAM4L means engineering teams can confidently balance the power budget, without compromising on performance.

Editor's Notes

About Atmel Corporation

Atmel Corporation (Nasdaq: ATML) is a worldwide leader in the design and manufacture of microcontrollers, capacitive touch solutions, advanced logic, mixed-signal, nonvolatile memory and radio frequency (RF) components. Leveraging one of the industry's broadest intellectual property (IP) technology portfolios, Atmel is able to provide the electronics industry with complete system solutions focused on industrial, consumer, communications, computing and automotive markets.Further information can be obtained from the Atmel website at www.atmel.com.

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